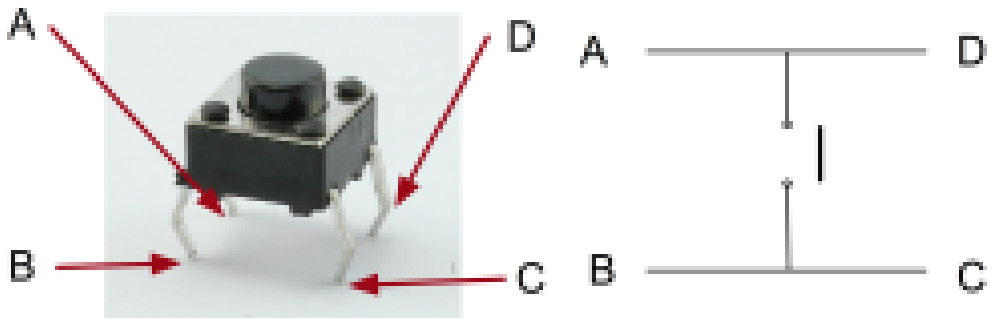
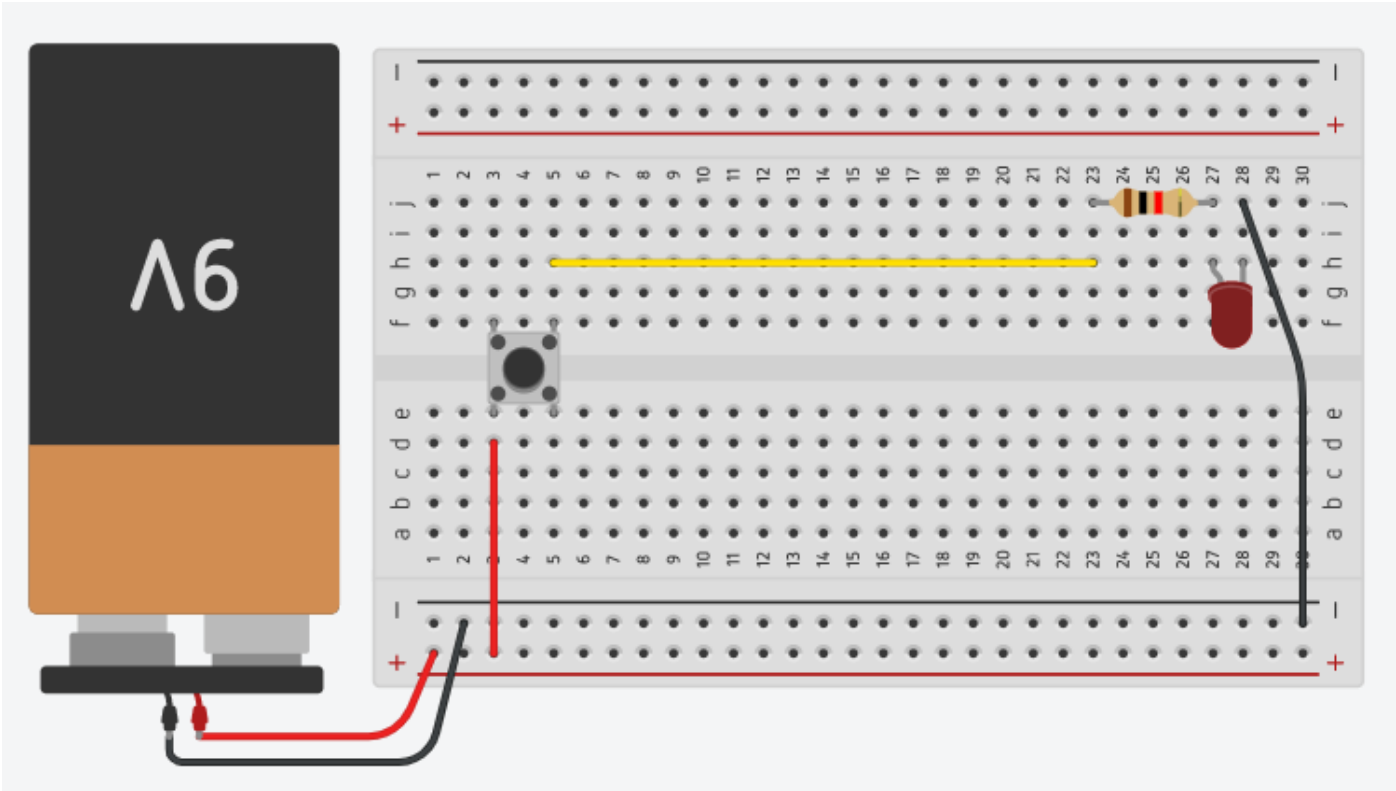
# Esercitazioni di sistemi classe III AME

## PORTE LOGICHE CON DIODI E TRANSISTOR

1- Simulare i circuiti assegnati con “ideal circuits” e ricavare la tabella della verità
2- Simulare i circuiti assegnati con “thinkercad”
3- Realizzare i circuiti su breadboard (lavorare a coppie sul banco)
4- Scrivere una relazione tecnica su quanto fatto.

### IL PUSH BUTTON

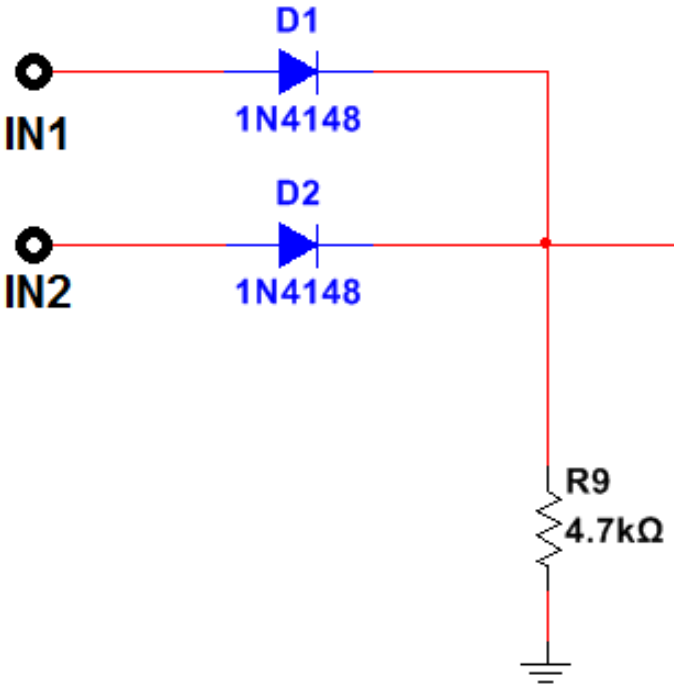


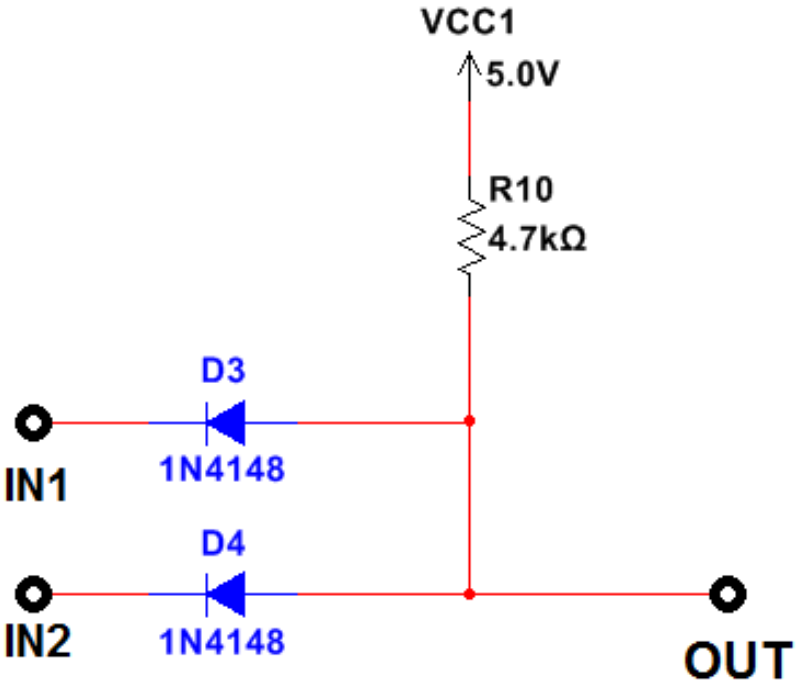
## Circuti assegnati

livello basso = 0 = GROUND = TERRA

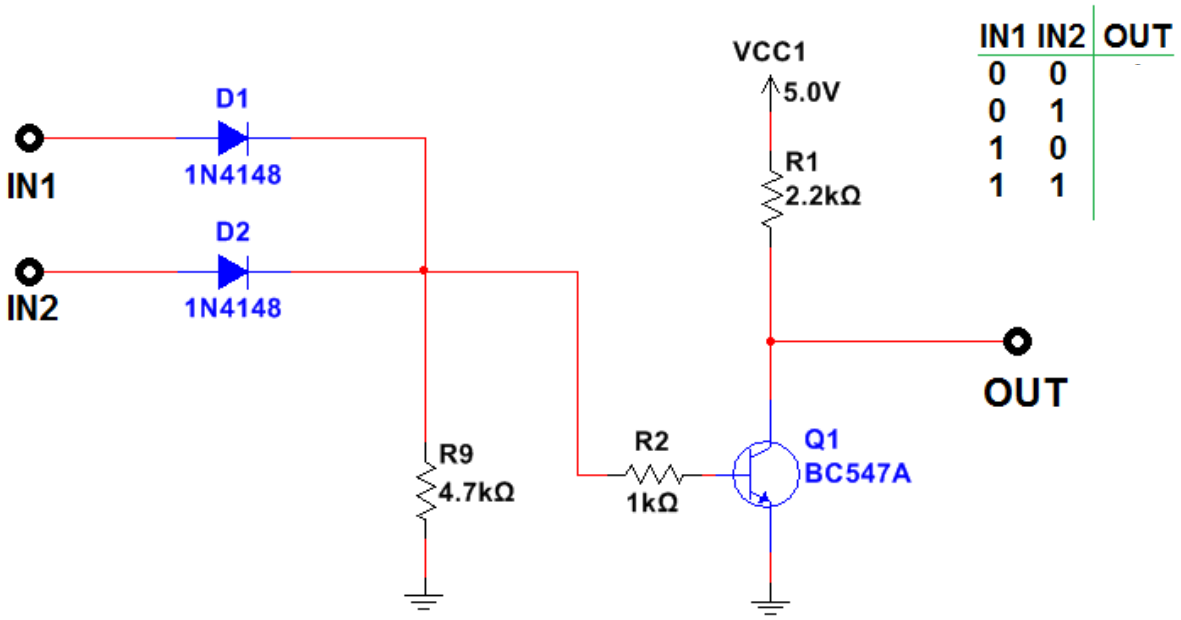
livello alto = 1 = Vcc = 5 volt



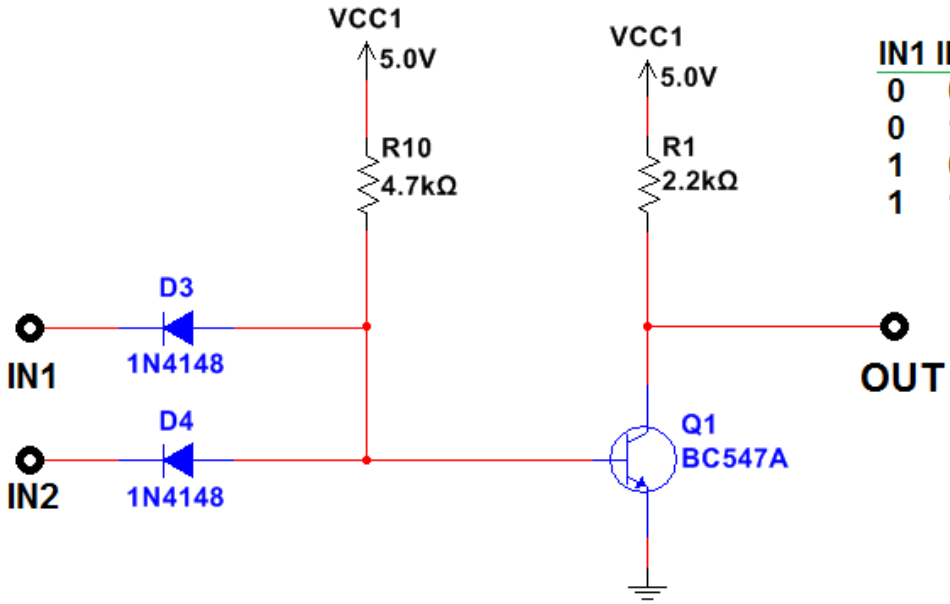

| IN1 | IN2 | OUT |
|---|---|---|
| 0 | 0 | |
| 0 | 1 | |
| 1 | 0 | |
| 1 | 1 | |



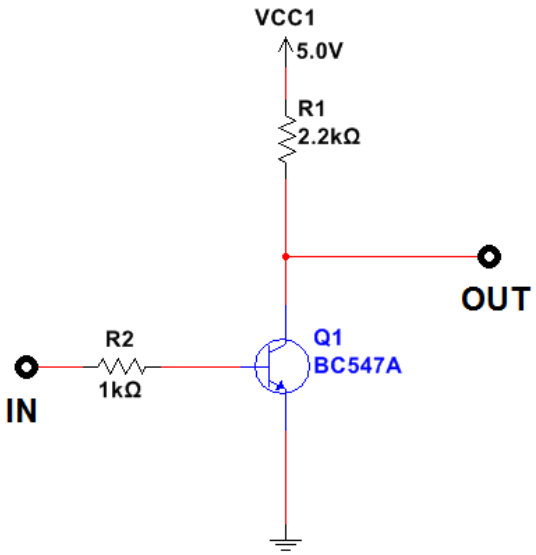

| IN1 | IN2 | OUT |
|---|---|---|
| 0 | 0 | |
| 0 | 1 | |
| 1 | 0 | |
| 1 | 1 | |

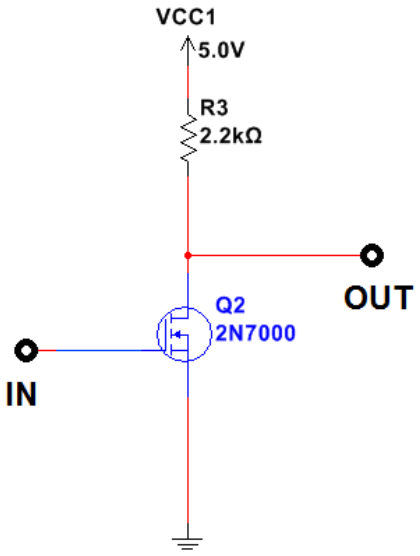


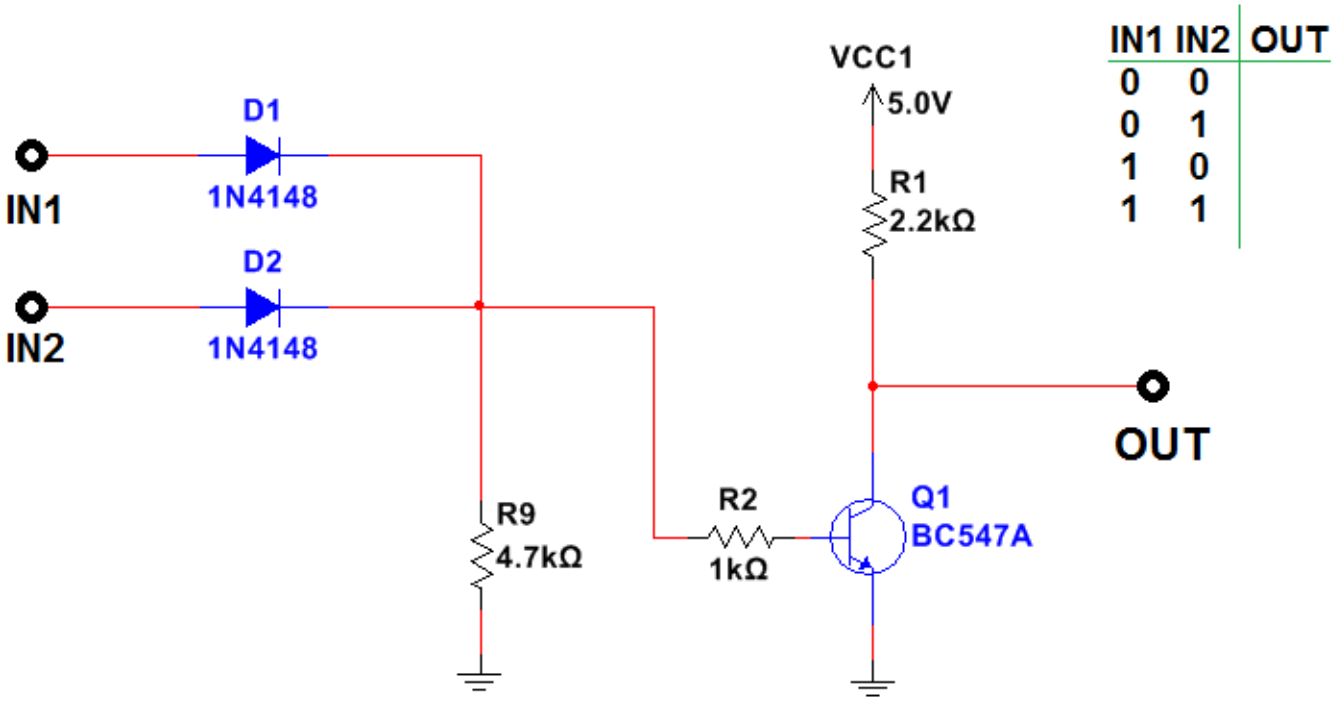

| IN1 | IN2 | OUT |
|---|---|---|
| 0 | 0 | |
| 0 | 1 | |
| 1 | 0 | |
| 1 | 1 | |



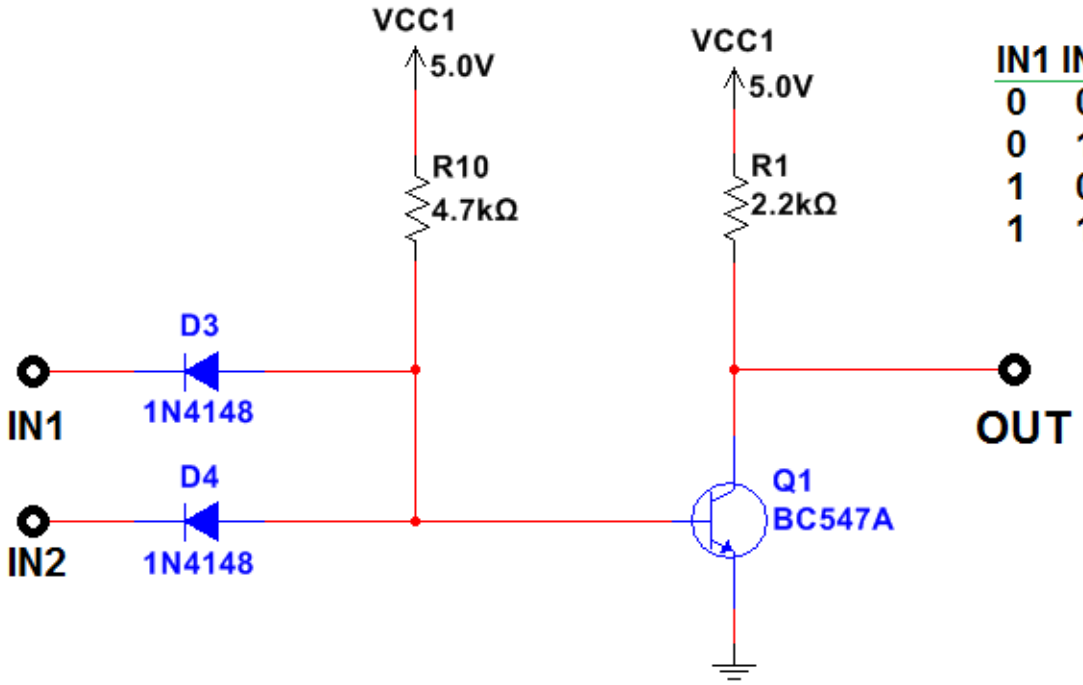

| IN1 | IN2 | OUT |
|---|---|---|
| 0 | 0 | |
| 0 | 1 | |
| 1 | 0 | |
| 1 | 1 | |



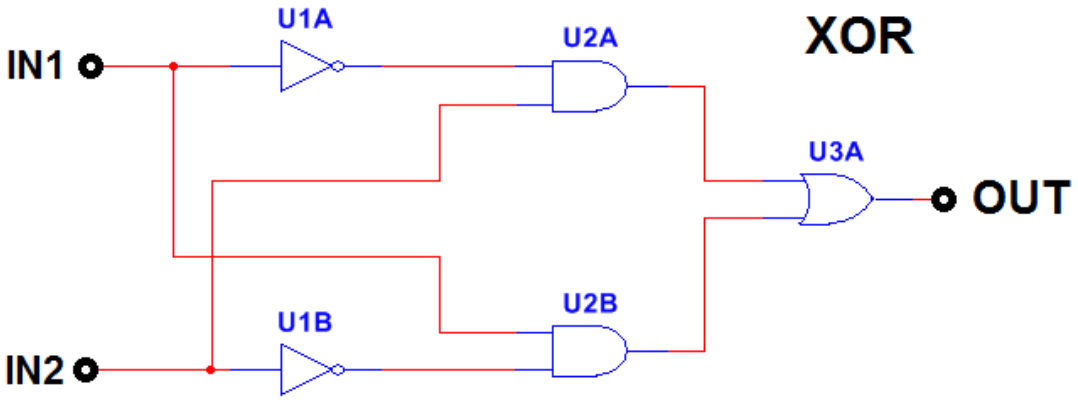



| IN1 | IN2 | OUT |
|---|---|---|
| 0 | 0 | |
| 0 | 1 | |
| 1 | 0 | |
| 1 | 1 | |

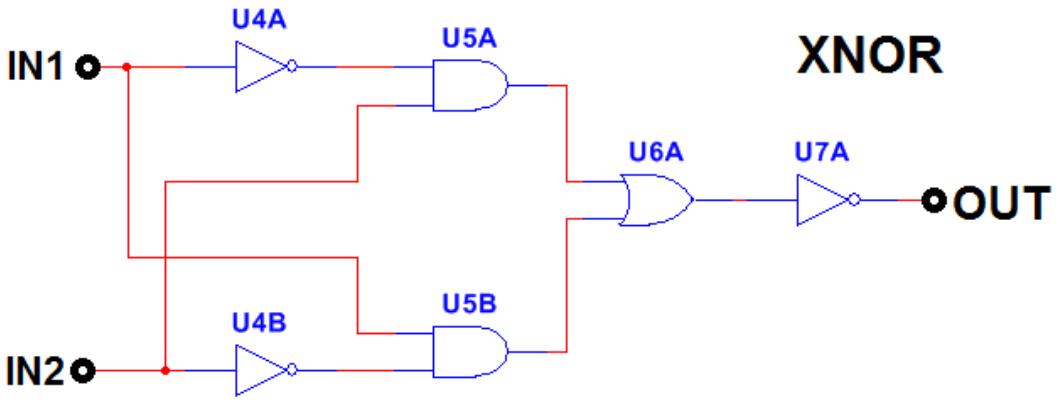



| IN1 | IN2 | OUT |
|---|---|---|
| 0 | 0 | |
| 0 | 1 | |
| 1 | 0 | |
| 1 | 1 | |

**Disegnare lo schema elettrico (con diodi e transistor) delle seguenti due porte e ricavare la tabella della verità**




| IN1 | IN2 | OUT |
|---|---|---|
| 0 | 0 | |
| 0 | 1 | |
| 1 | 0 | |
| 1 | 1 | |

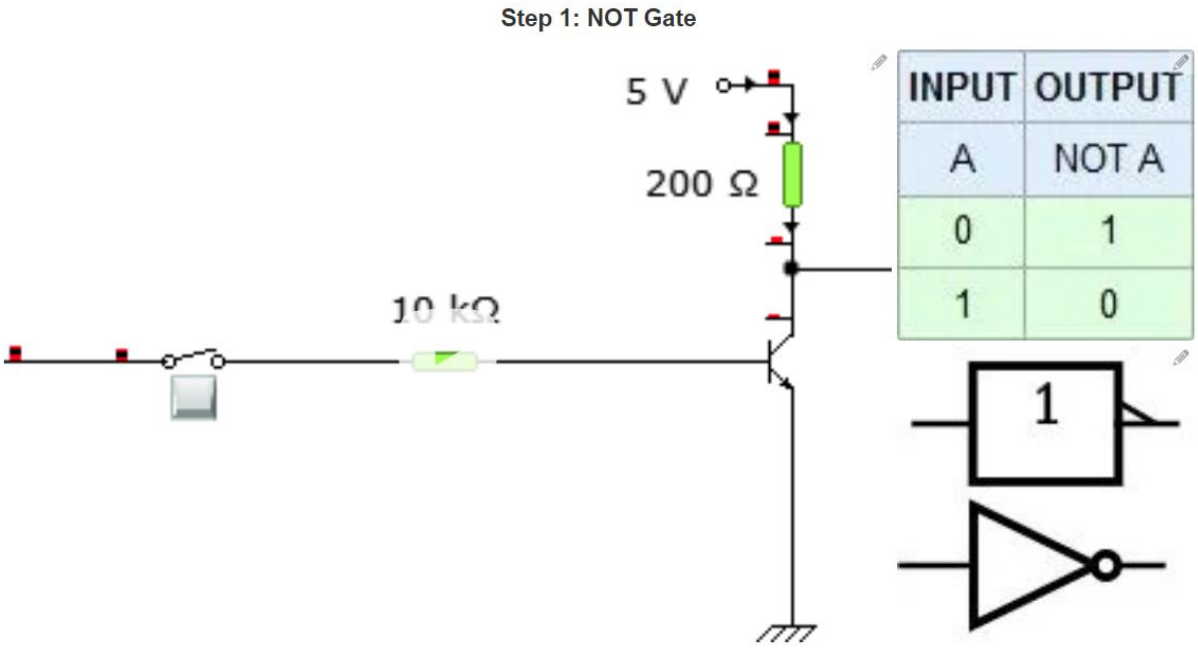



| IN1 | IN2 | OUT |
|---|---|---|
| 0 | 0 | |
| 0 | 1 | |
| 1 | 0 | |
| 1 | 1 | |

# PORTE LOGICHE CON SOLI TRANSISTORS

1- Simulare i circuiti assegnati con “ideal circuits” e ricavare la tabella della verità
2- Simulare i circuiti assegnati con “thinkercad”
3- Realizzare i circuiti su breadboard (lavorare a coppie sul banco)
4- Scrivere una relazione tecnica su quanto fatto.

# PORTA NOT

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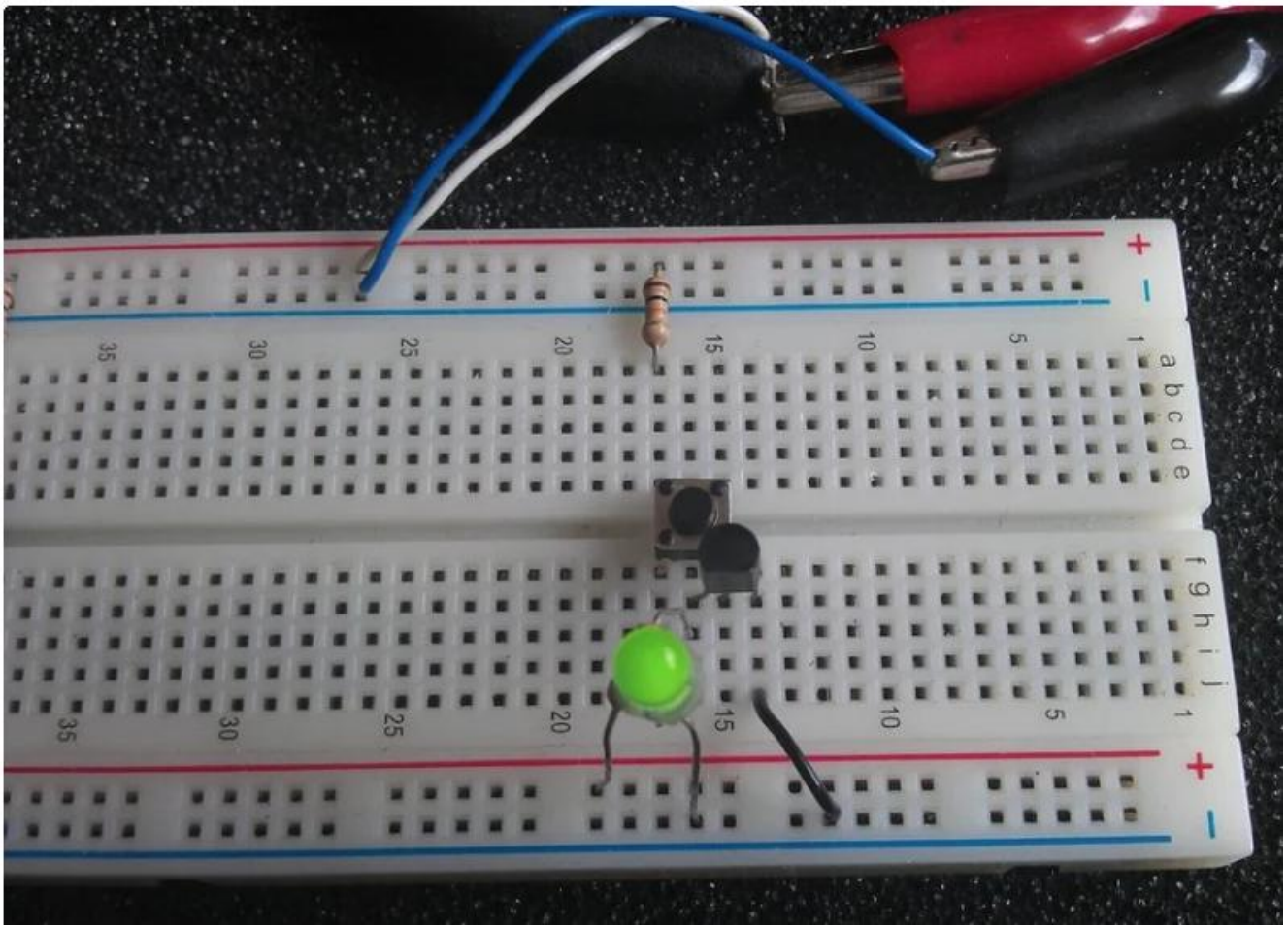
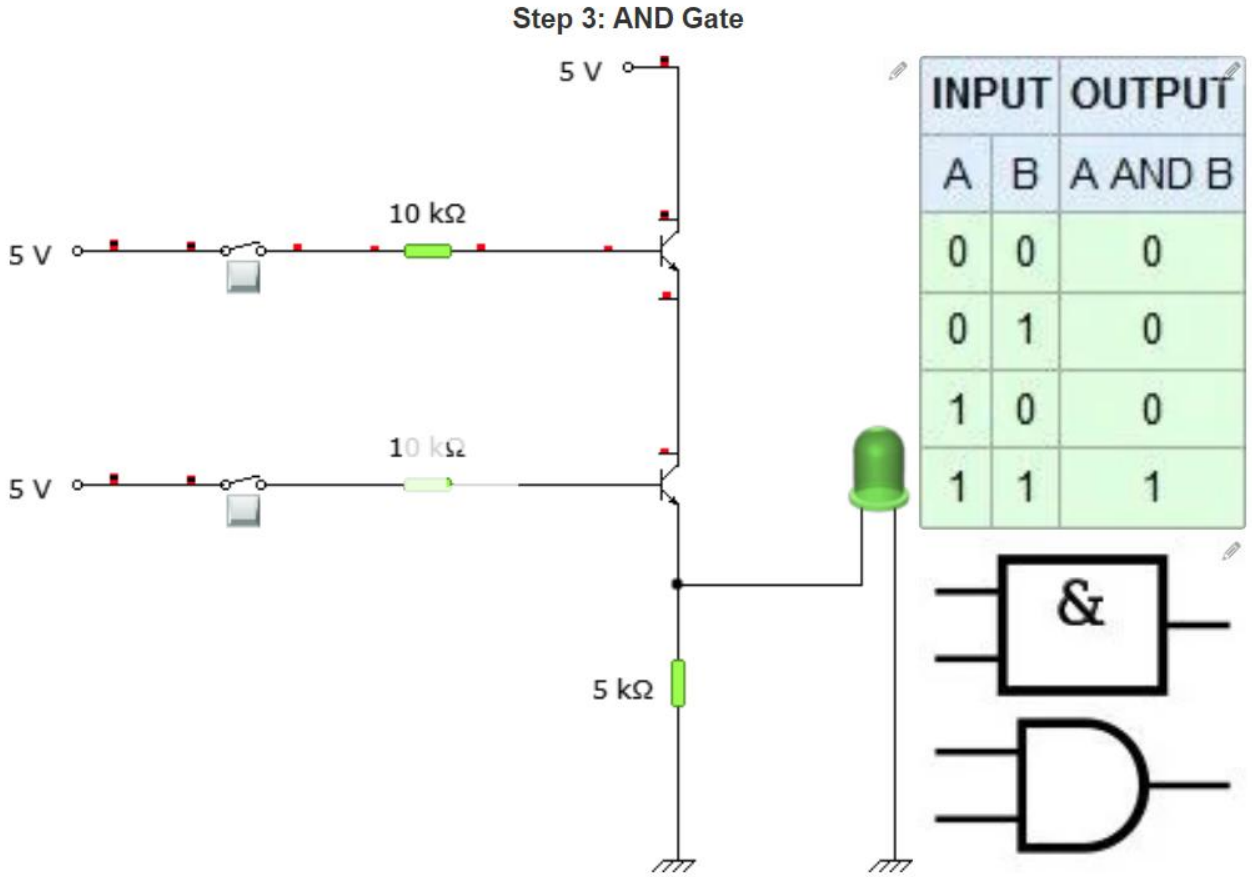
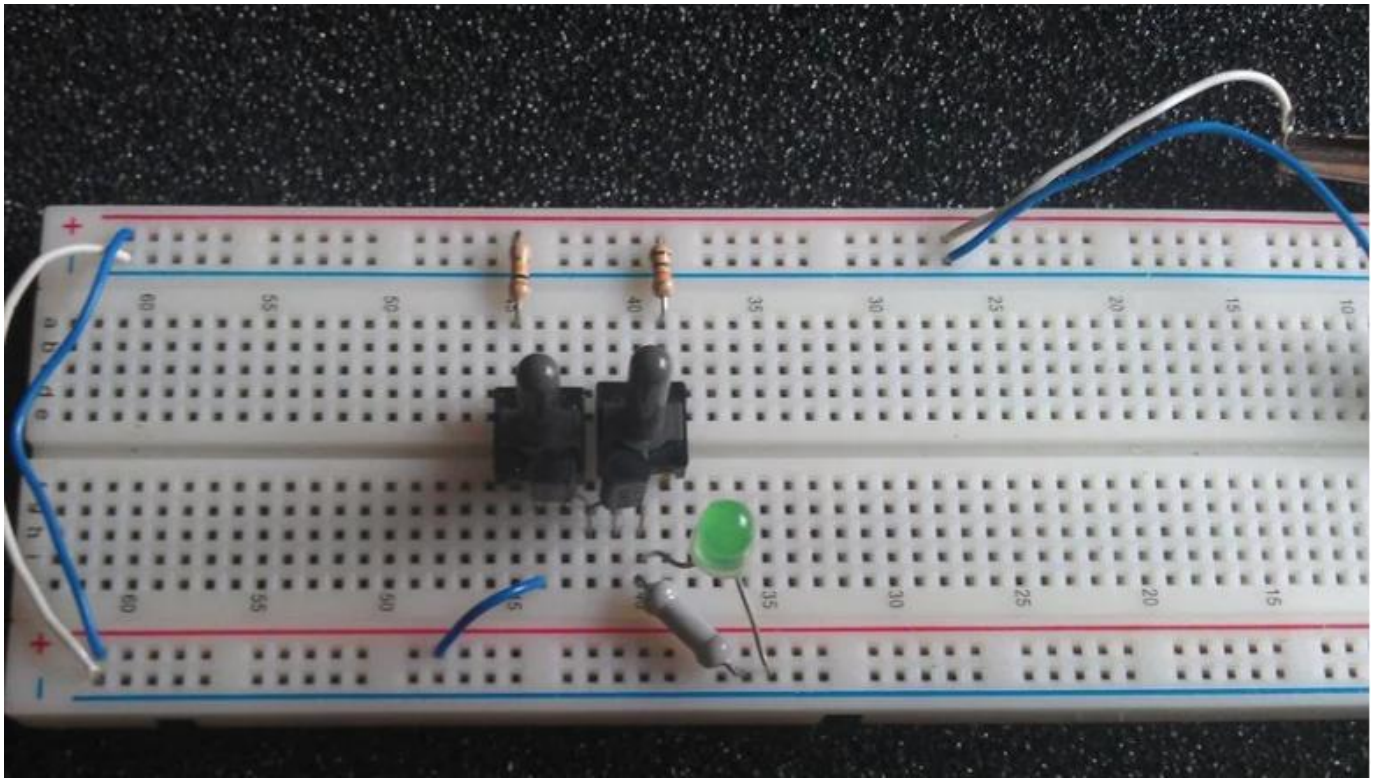
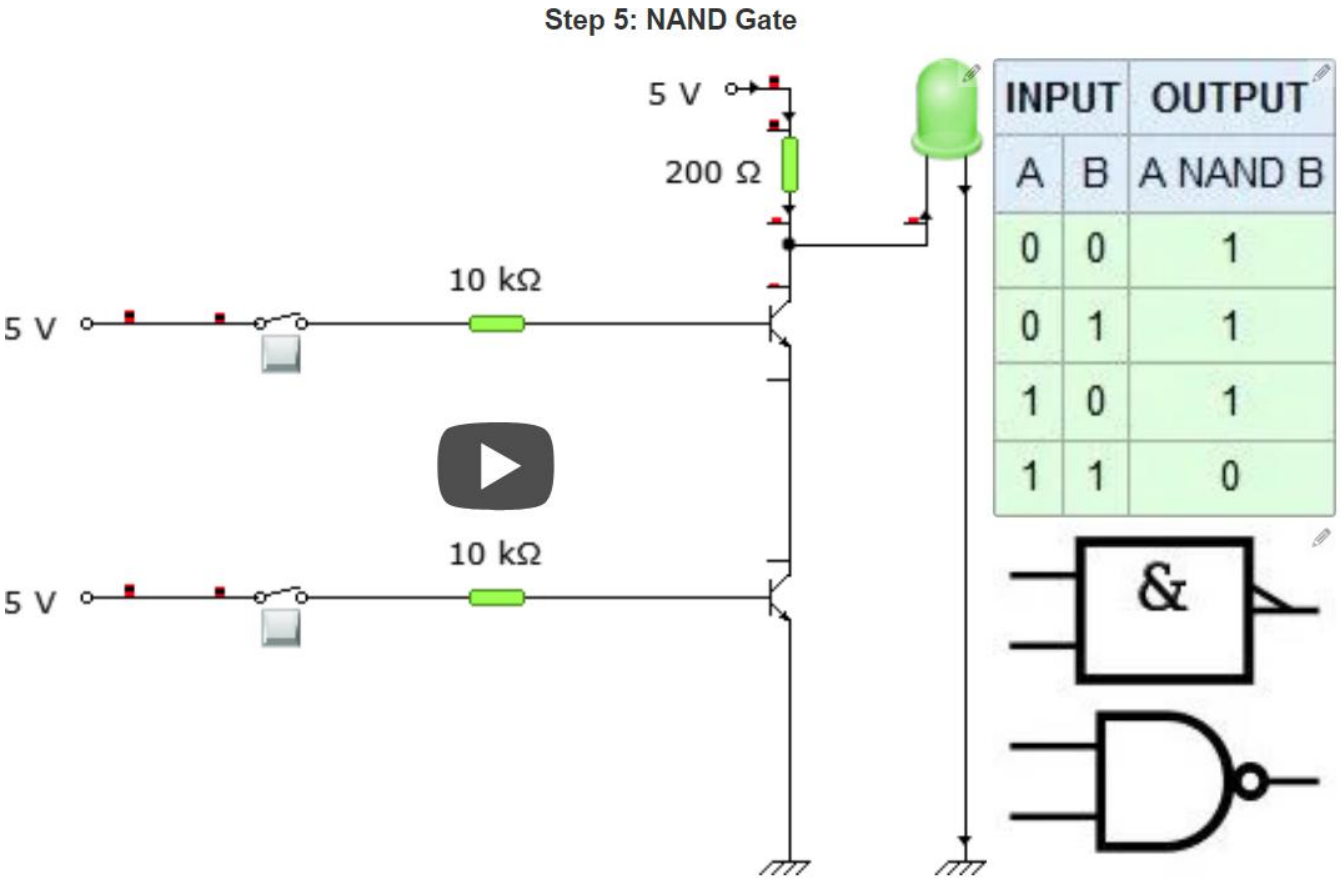


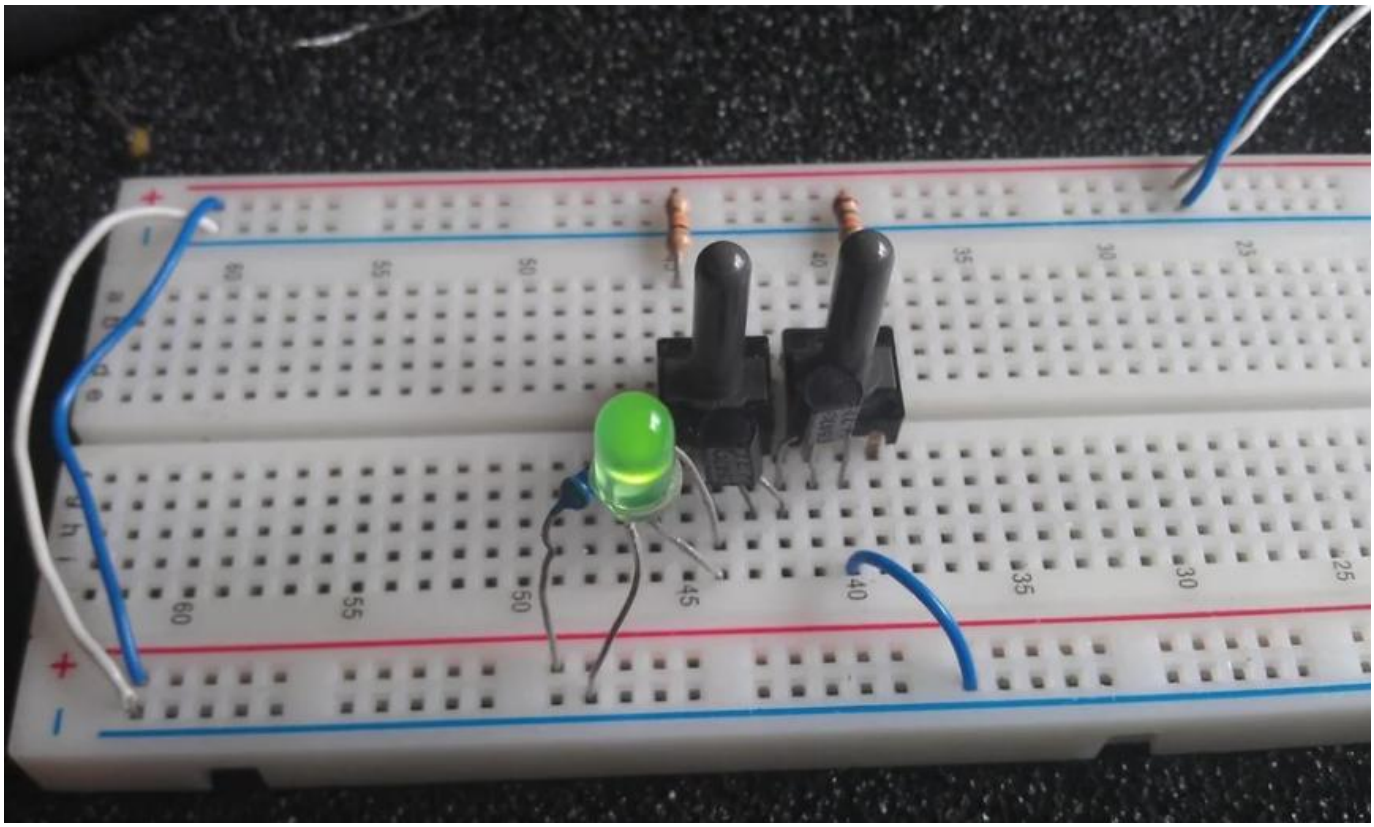
# PORTA AND


Step 3: AND Gate
5 V
10 kΩ
5 V
10 kΩ
5 V
5 kΩ
INPUT
OUTPUT
A
B
A AND B
0 0 0
0 1 0
1 0 0
1 1 1
&

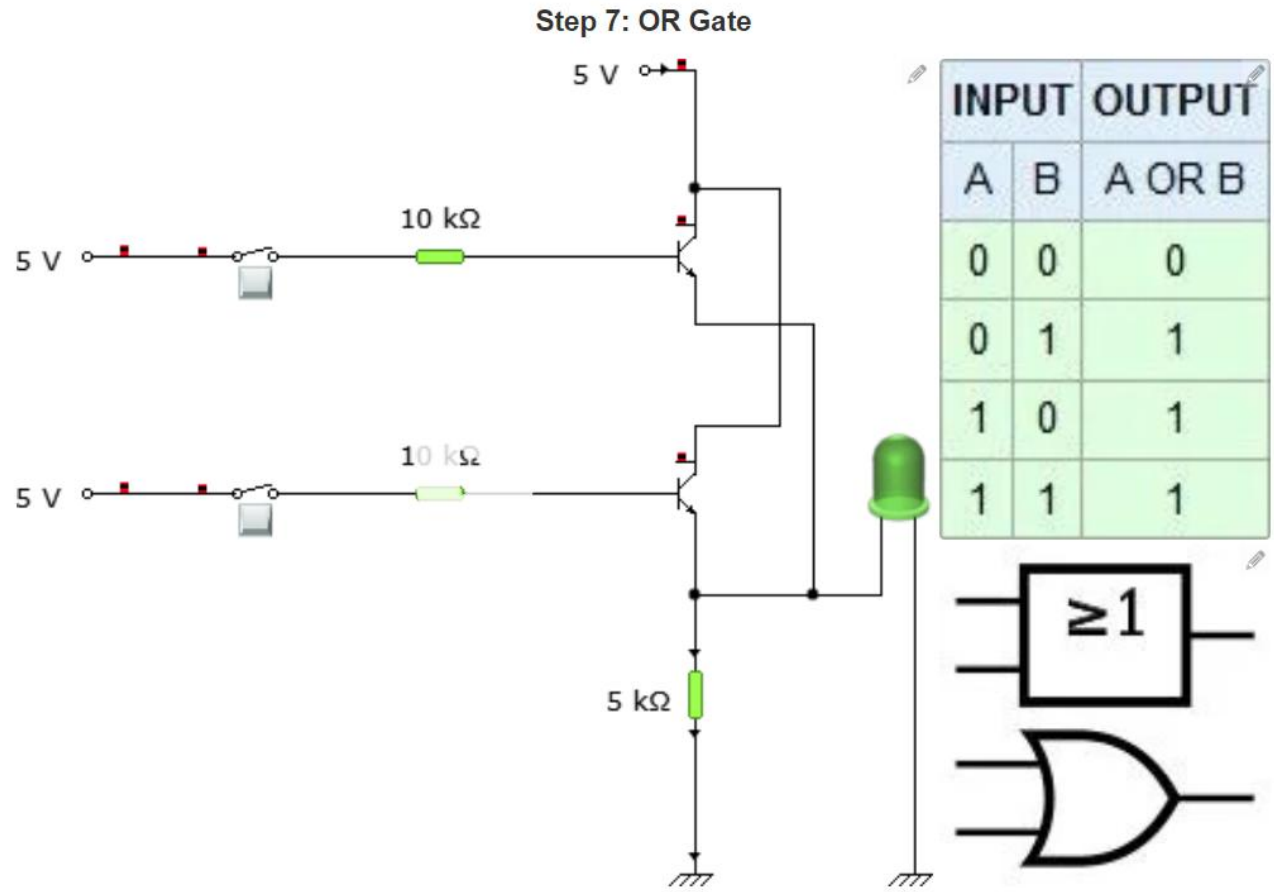


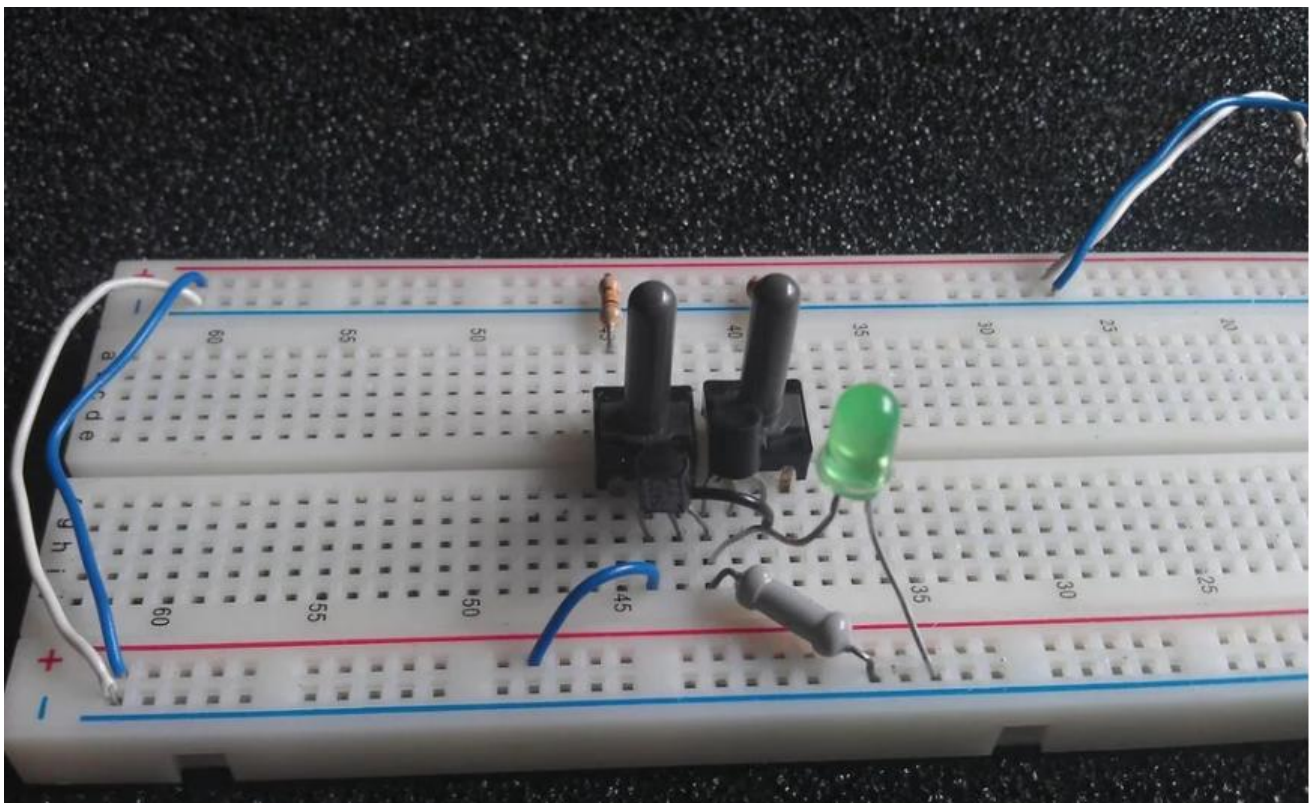
# PORTA NAND


Step 5: NAND Gate
5 V
200 Ω
10 kΩ
5 V
10 kΩ
5 V
INPUT
OUTPUT
A
B
A NAND B
0 0 1
0 1 1
1 0 1
1 1 0
&

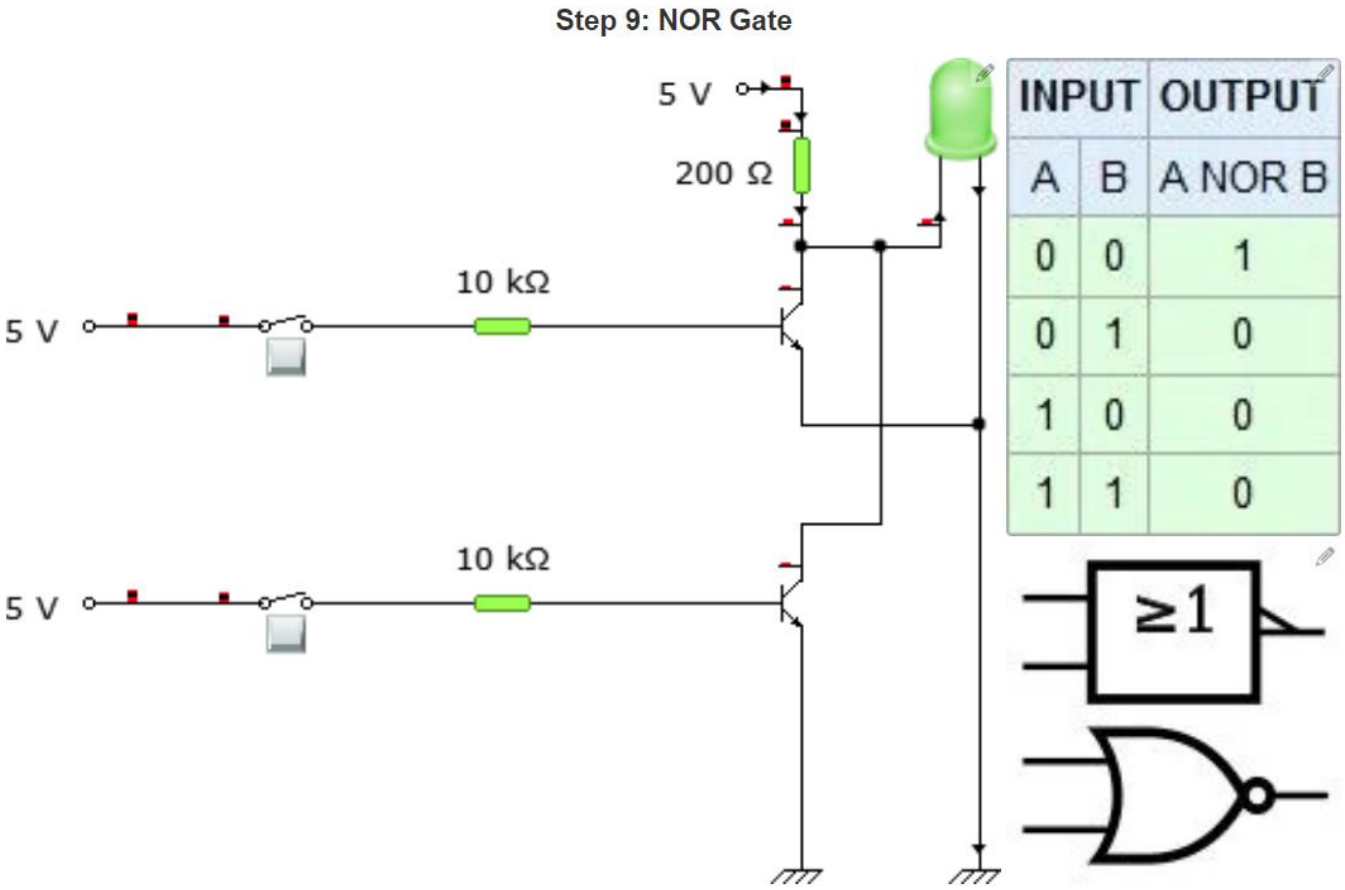


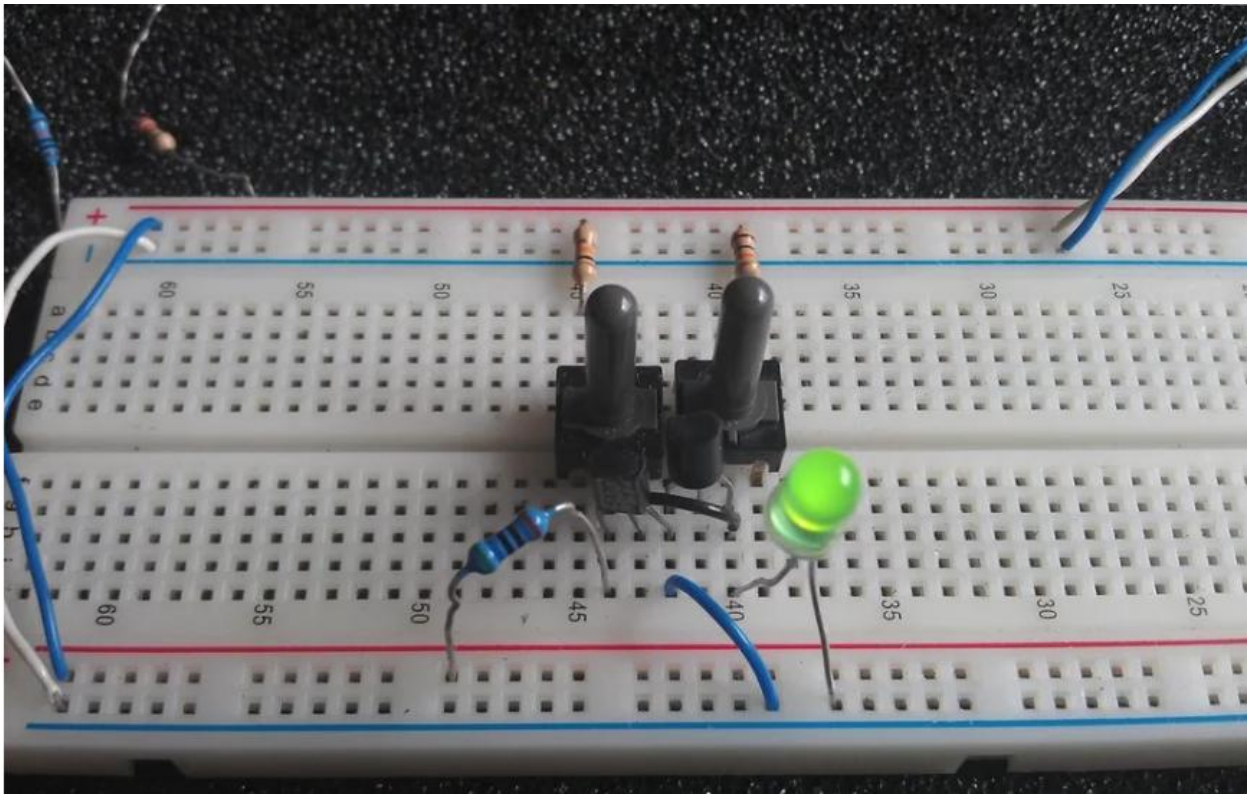
# PORTA OR


Step 7: OR Gate
5 V
10 kΩ
5 V
10 kΩ
5 V
5 kΩ
INPUT
OUTPUT
A
B
A OR B
0 0 0
0 1 1
1 0 1
1 1 1
≥1



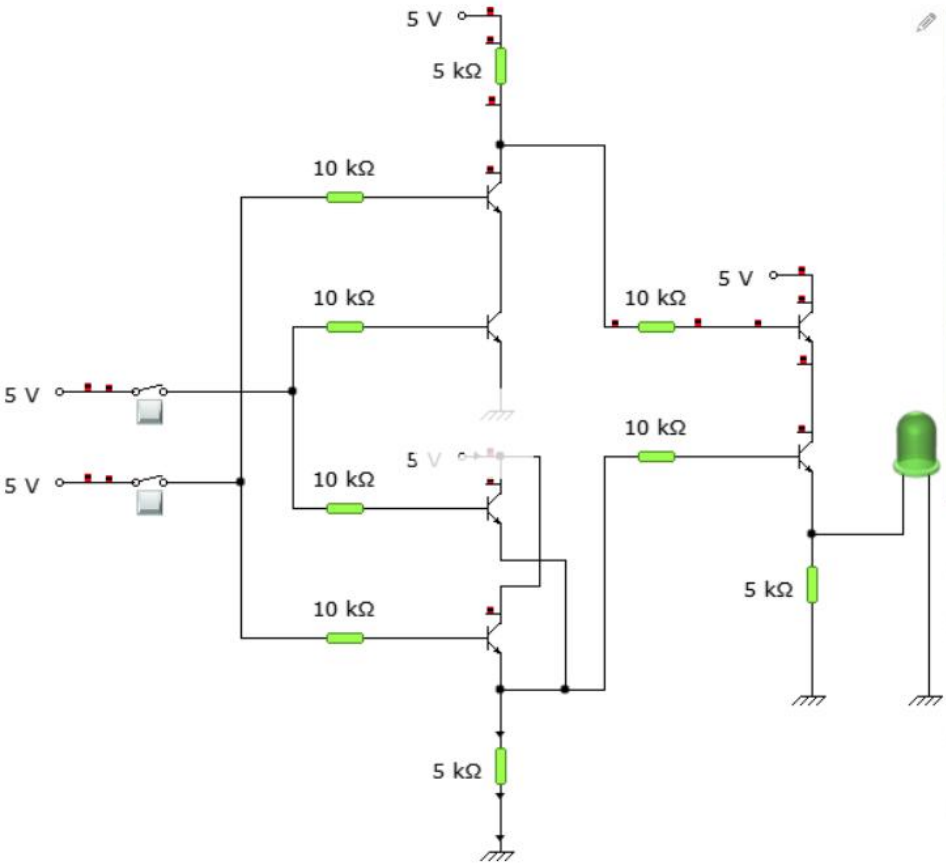
# PORTA NOR


Step 9: NOR Gate
5 V
200 Ω
10 kΩ
5 V
10 kΩ
5 V
INPUT
OUTPUT
A
B
A NOR B
0 0 1
0 1 0
1 0 0
1 1 0
≥1

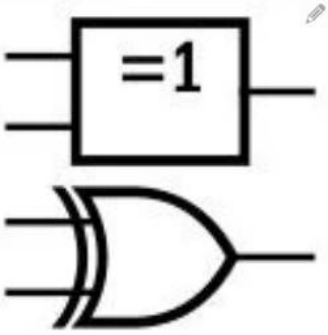


# PORTA XOR e XNOR

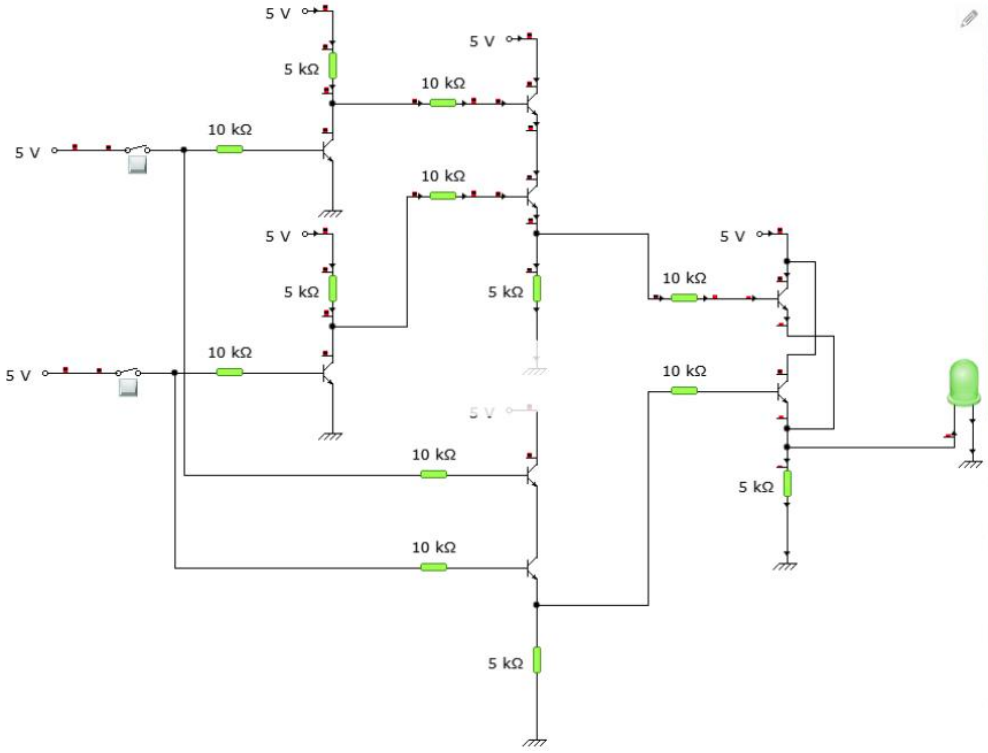
## Step 11: XOR Gate



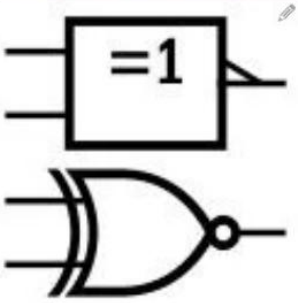

| INPUT | | OUTPUT |
|---|---|---|
| A | B | A XOR B |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |




## Step 12: XNOR Gate

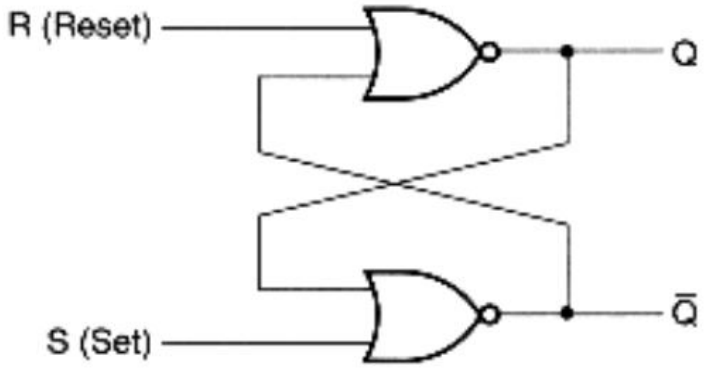



| INPUT | | OUTPUT |
|---|---|---|
| A | B | A XNOR B |
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |



# Le memorie SR

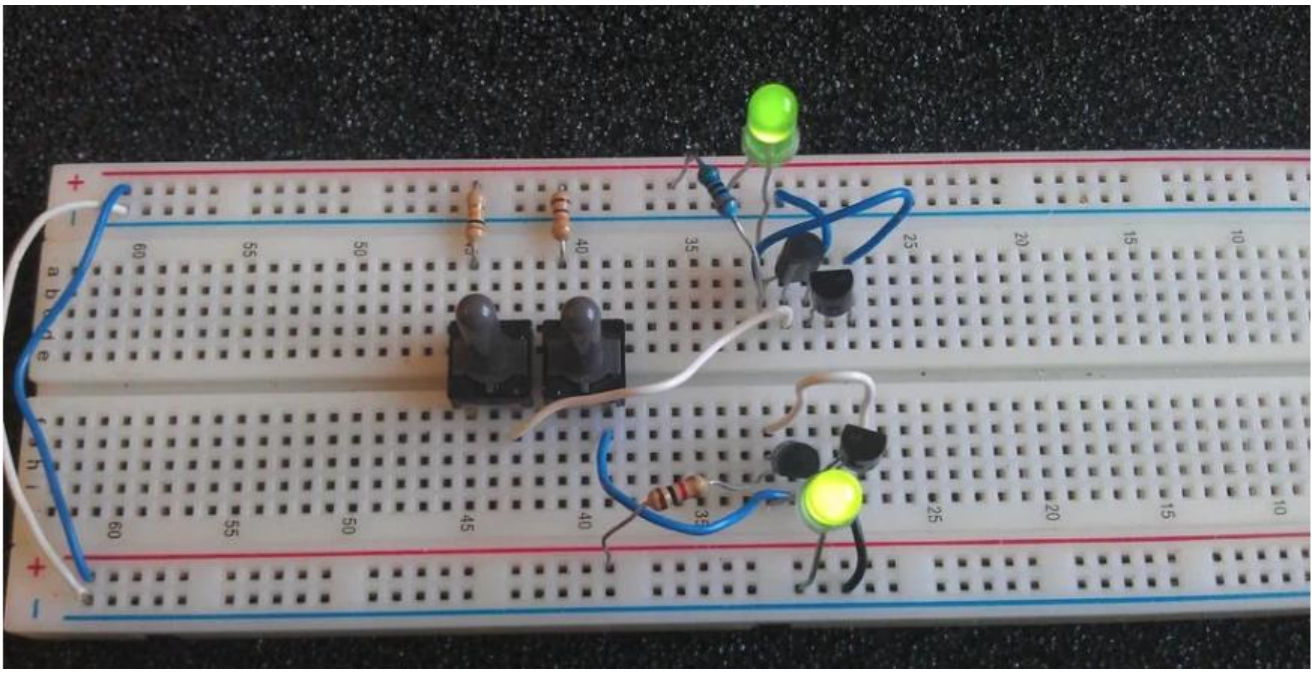
**Step 13: Build Something! - SR Flip-flop**




(a) Logic diagram

| S | R | Q | $\overline{Q}$ | |
|---|---|---|---|---|
| 1 | 0 | 1 | 0 | Set state |
| 0 | 0 | 1 | 0 | |
| 0 | 1 | 0 | 1 | Reset state |
| 0 | 0 | 0 | 1 | |
| 1 | 1 | 0 | 0 | Undefined |

(b) Function table



When using static gates as building blocks, the most fundamental latch is the simple SR latch, where S and R stand for set and reset. It can be constructed from a pair of cross-coupled NOR logic gates. The stored bit is present on the output marked Q.
The output usually marked as Q, but sometimes it is marked as X, Y or F.

While the S and R inputs are both low, feedback maintains the Q and Q' outputs in a constant state, with Q' the complement of Q. If S (Set) is pulsed high (=when you push the button) while R (Reset) is held low, then the Q output is forced high, and stays high when S returns to low; similarly, if R is pulsed high while S is held low, then the Q output is forced low, and stays low when R returns to low.